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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,571	12/03/2003	Masafumi Asano	03180.0343	5144

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EXAMINER	
ROSASCO, STEPHEN D	
ART UNIT	**PAPER NUMBER**
1756	

DATE MAILED: 02/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,571	ASANO ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *11-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/03/03; 2,8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Applicant's election without traverse of Group I (claims 1-10) in the reply filed on 11/28/05 is acknowledged.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticiapted by Spence (5,702,848).

The claimed invention is directed to a reticle set, comprising: a first photomask having a circuit pattern provided with first and second openings provided adjacent to each other sandwiching a first opaque portion, and a monitor mark provided adjacent to the circuit pattern; and a second photomask having a trim pattern provided with a second opaque portion configured to cover the first opaque portion in an area occupied by the circuit pattern and an extending portion connected to one end of the first opaque portion and configured to extend outside the area occupied by the circuit pattern when the second photomask is aligned with a pattern delineated on a substrate by the first photomask.

And wherein phases of an exposure light transmitting through the first and second openings are shifted by 180 degrees from each other.

And wherein a part of the monitor mark is provided at a corresponding position where another circuit pattern is to be delineated on the substrate in another exposure process.

And wherein the monitor mark includes at least one of an exposure monitor mark configured to measure an exposure condition of the first photomask and an inspection monitor mark for a photomask.

And wherein the exposure monitor mark includes at least one of a dimension monitor mark configured to monitor a dimension of a transferred pattern on the substrate, an exposure dose monitor mark configured to monitor an exposure dose, and an alignment mark configured to monitor a displacement of the transferred pattern.

The applicant discusses the limitations of the prior art in that in a reticle set on which a high density semiconductor circuit pattern has been delineated, the monitor marks are disposed only in limited are as such as scribe lines because of restrictions on layout. Accordingly, in an actual semiconductor integrated circuit manufacturing process, it is difficult to acquire detailed information on positions and dimensions over the entire exposure area.

Spence teaches an integrated circuit (IC) being formed from an i-line stepper lithography method for phase shift mask patterning for forming the levels of the IC on a semiconductor wafer, said lithography method including use of different masks to pattern the layout of different levels, one such level being the gate level and a second such level being the active regions, said active regions being spatially defined by an active region layout pattern, said gate level being spatially defined by a gate level pattern having first and second gate level layout portions, said first gate level layout portion being a standard non-phase shift mask pattern having opaque and non-opaque regions and said second gate level layout portion having areas containing phase shift regions, wherein said method comrises the steps of: providing on said phase shift mask a compensating transition phase shift region around and contiguous to said 180 degree phase shift regions and between said 180 degree phase shift regions and said zero phase

regions, said compensating transition phase shift region being contiguous with the entire periphery of said 180 degree phase area except for the region where said 180 degree phase area overlaps a region having said opaque pattern thereon.

And wherein said 180 degree phase shift regions are etched regions of said PSM providing a leading phase of said light which transmits through said 180 degree phase shift region relative to the phase of said light which does not pass through said 180 degree phase shift region.

And wherein the method further comprises the steps of: constructing a trim mask having a dark field surrounding a transmission pattern, said transmission pattern being a pattern having a center line which exactly corresponds to the locus of some of transitions between a zero degree to 180 degree regions; before the step of developing said exposed positive resist, again exposing said positive resist on said integrated circuit with a partially coherent light source directed through said trim mask which trim mask has been aligned so that the zero to 180 degree locus of said trim mask is aligned with said 0/180 degree transitions regions exposed during said first exposure.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Miniami et al. (6,773,853) or Wang et al. (6,566,023).

The claimed invention is directed to a reticle set, comprising: a first photomask having a circuit pattern provided with first and second openings provided adjacent to each other sandwiching a first opaque portion, and a monitor mark provided adjacent to the circuit pattern; and a second photomask having a trim pattern provided with a second opaque portion configured to cover the first opaque portion in an area occupied by the circuit pattern and an extending portion connected to one end of the first opaque portion and configured to extend outside the area occupied by the circuit pattern when the second photomask is aligned with a pattern delineated on a substrate by the first photomask.

And wherein phases of an exposure light transmitting through the first and second openings are shifted by 180 degrees from each other.

And wherein a part of the monitor mark is provided at a corresponding position where another circuit pattern is to be delineated on the substrate in another exposure process.

And wherein the monitor mark includes at least one of an exposure monitor mark configured to measure an exposure condition of the first photomask and an inspection monitor mark for a photomask.

And wherein the exposure monitor mark includes at least one of a dimension monitor mark configured to monitor a dimension of a transferred pattern on the substrate, an exposure dose monitor mark configured to monitor an exposure dose, and an alignment mark configured to monitor a displacement of the transferred pattern.

The applicant discusses the limitations of the prior art in that in a reticle set on which a high density semiconductor circuit pattern has been delineated, the monitor marks are disposed only in limited are as such as scribe lines because of restrictions on layout. Accordingly, in an actual semiconductor integrated circuit manufacturing process, it is difficult to acquire detailed information on positions and dimensions over the entire exposure area.

Minami et al. teach a reticle set for semiconductor device manufacture, comprising: first and second reticles for exposing one layer formed on a substrate having a plurality of sections defined on a surface of the substrate, each section being exposed by one shot, an outer peripheral area of each section overlapping an outer peripheral area of a section adjacent to the first-mentioned section, this overlap area corresponding to a scribe line; and wherein: when a first section among first and second sections adjacent to each other is exposed, each of mark areas of the first and second reticles corresponds to the scribe line corresponding to the overlap area of the first and second sections, when the second section is exposed, each of margin areas of the first and second reticles corresponds to the scribe line corresponding to the overlap area of the first and second sections; a fifth mark is disposed in the mark area of the second reticle; and an area of the mark area of the first reticle corresponding to an area including a pattern transferred from the fifth mark on the substrate is a partial transmission area for partially transmitting exposure light.

And wherein an area of the margin area of the first reticle corresponding to an area including the pattern, on the substrate, transferred from the fifth mark is a light-shielding area.

And wherein a sixth mark is formed in the partial transmission area in the mark area of the first reticle, the sixth mark being used for transferring a pattern for testing a placement error from the pattern transferred from the fifth mark.

Wang et al. teach a mask set and a method for manufacturing a set of masks, comprising: reading a layout file for a mask set designed for integrated circuit components having first critical dimensions; creating phase shift mask layout file having phase shift areas in respective openings in an opaque field to shrink the first critical dimensions to second critical dimensions for particular components of the integrated circuit components in a layer of material

to define active regions having the second critical dimensions, the phase shifting areas include a first phase shift area, and a second phase shift area, where destructive interference occurs between said first phase shift area and said second phase shift area, and wherein said first phase shift area is aligned with said respective opening in said opaque field by a phase shift mask overlap area; and creating a second mask layout file defining other structure in said layer; and manufacturing at least one mask using the phase shift mask layout file and the trim mask layout file.

And wherein said first phase shift area has a relative phase shift of theta degrees and said second phase shift area has a relative phase shift of approximately theta +180 degrees.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
1/26/06